WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit apparatus for communication, comprising:

a buffer in which input data is written by a write clock based on an input clock concerned with the input data and from which the written data is read out by a read clock;

clock switching means for selecting either said input clock or a stable external clock which is supplied from an outside on the basis of a selection signal from the outside; and

a circuit for producing the read clock on the basis of an output of said clock switching means,

wherein said read clock producing circuit includes

a PLL circuit for receiving the output of said clock switching means and generating a PLL clock locked with said output and a frequency divider for frequency dividing said PLL clock and generating said read clock.

2. An apparatus according to claim 1, further comprising a write clock producing circuit which can produce said write clock in response to a control signal from the outside and a clock signal based on said PLL clock when the stable external clock which is supplied from said outside is selected by said clock switching means.

3. An apparatus according to claim 2, further

comprising a detector for comparing a phase of said write clock from said write clock producing circuit with that of said read clock from said read clock producing circuit and generating a detection signal showing that a phase difference between them is equal to or larger than a predetermined value,

and wherein the control signal from said outside is supplied to said semiconductor integrated circuit apparatus in response to said detection signal.

4. An apparatus according to claim 1, wherein said PLL circuit has a first PLL circuit section for receiving the output of said clock switching means and generating an intermediate reference clock and a second PLL circuit section for receiving said intermediate reference clock and generating said PLL clock, said first PLL circuit section has an externally attached voltage controlled oscillator, and said second PLL circuit section has no externally attached device.

5. An apparatus according to claim 1, wherein said buffer has a construction adapted to transfer serial data of a plurality of channels and said apparatus further has a multiplexer for multiplexing the serial data of said plurality of channels read out from said buffer.

6. A semiconductor integrated circuit apparatus for correctly transferring received data formed with a single semiconductor chip, comprising:

an input data port for receiving input data

to the device;

an input clock port for receiving a data fetch clock related to said input data;

an external clock port for receiving a stabilized clock externally of said chip;

a control signal port for receiving a control signal externally of said chip;

an output data port;

a buffer to which the received input data is written with a write clock and from which the written data is read with a read clock for delivery to said output data port, said write clock being normally based on said data fetch clock and being made active or inactive by a control signal received at said control signal port; and

a clock producing circuit for determining said read clock, the clock producing circuit including

a selector for receiving a portion of said data fetch clock from said input clock port and said stabilized clock from said external clock port and passing one of said data fetch clock and stabilized clock as an output, and

a PLL connected to receive the output of said selector and generate a PLL clock locked to said output of said selector, said read clock being based on said PLL clock.

7. A semiconductor integrated circuit apparatus according to claim 6, wherein said PLL includes a first

PLL section for generating an intermediary reference clock from said output of said selector and a second PLL section for generating said PLL clock from said intermediary clock, said first PLL section being connected to an oscillator connection port for external connection with a voltage-controlled oscillator, said second PLL having no externally connected element.

8. A semiconductor integrated circuit apparatus for correctly transferring received data formed with a single semiconductor chip, comprising:

an input data port for receiving input data to the device;

an input clock port for receiving a data fetch clock related to said input data;

an external clock port for receiving a stabilized clock externally of said chip;

a control signal port for receiving an external control signal externally of said chip;

a detection signal port;

an output data port;

a buffer to which the received input data is written with a write clock and from which the written data is read with a read clock for delivery to said output data port; and

a clock producing circuit for determining said write clock and said read clock, the clock producing circuit including

means connected to receive said data fetch

clock from said input clock port and receive said external control signal from said control signal port for generating from said data fetch clock said write clock under control of said external control signal,

a selector for receiving said write clock from said write clock generating means and said stabilized clock from said external clock port and passing one of said write clock and said stabilized clock as an output,

a PLL connected to receive the output of said selector and generate a PLL clock locked to said output of said selector,

means connected to receive said PLL clock from said PLL for generating therefrom said read clock, and

a detector electrically connected to receive another portion of said write clock from said write clock generating means and a portion of said read clock from said read clock generating means to phase-compare said write clock and read clock for generating, based on a phase comparison result, an internal control signal to be fed to said detection signal port,

said external control signal being supplied to said control signal port responsive to said internal control signal for control of said write clock to make it active or inactive.

9. A semiconductor integrated circuit apparatus according to claim 8, wherein said PLL includes a first

PLL section for generating an intermediary reference clock from said output of said selector and a second PLL section for generating said PLL clock from said intermediary clock, said first PLL section being connected to an oscillator connection port for external connection with a voltage-controlled oscillator, said second PLL having no externally connected element.

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